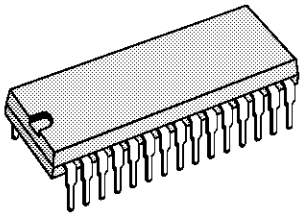
SGS-THOMSON MICROELECTRONICS

STV2100

PAL LUMA-CHROMA & DEFLECTION PROCESSOR

PRELIMINAY DATA

- FEW EXTERNAL COMPONENTS
- RGB AND FAST BLANKING INPUTS
- DC-CONTROLLED BRIGHTNESS, CONTRAST AND SATURATION
- CERAMIC 500kHz VCO FOR LINE DEFLECTION
- NO LINE AND FRAME OSCILLATOR ADJUSTMENTS REQUIRED
- PHASE-LOCKED REFERENCE OSCILLATOR USING A STANDARD 4.43MHz QUARTZ
- OSD CAPABILITY ON OUTPUTS
- VIDEO IDENTIFICATION GENERATOR



SHRINK DIP30
(plastic package)

ORDER CODE : STV2100

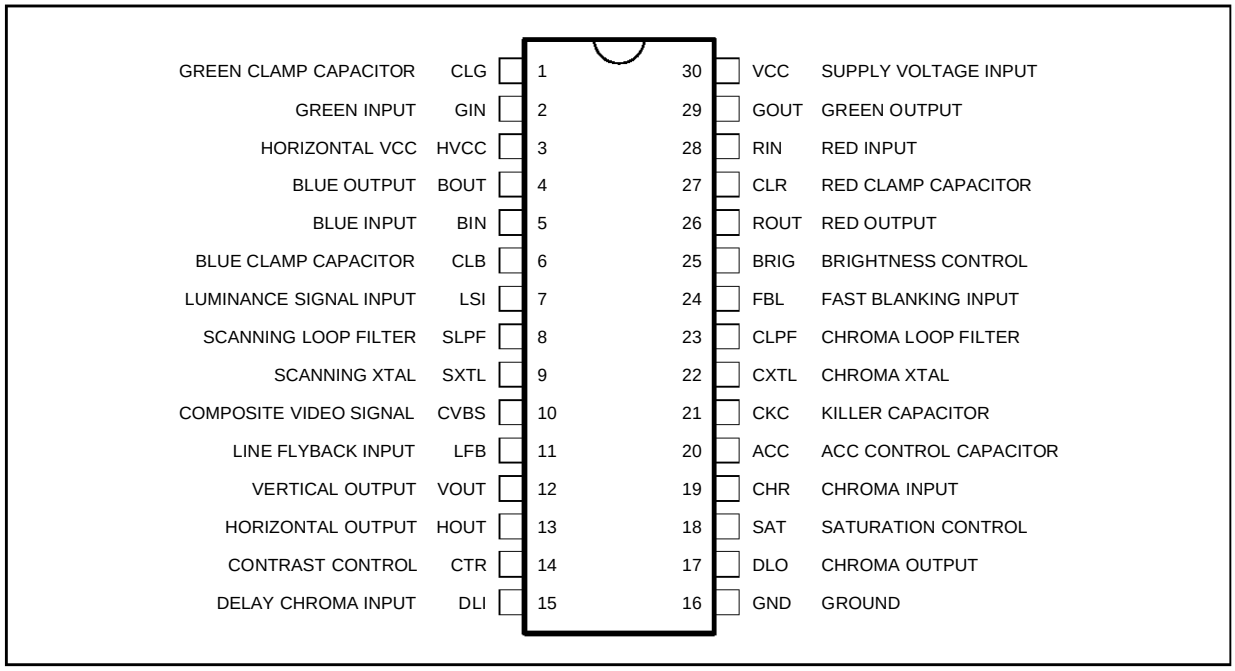
DESCRIPTION

The STV2100 is a PAL chroma decoder, video and H/V deflection processor for CTV.

Used with the TDA8222, this IC permits a complete low cost solution with external output stages.

The pin connection allows board compatibility with the PAL/SECAM processor STV2110.

PIN CONNECTIONS



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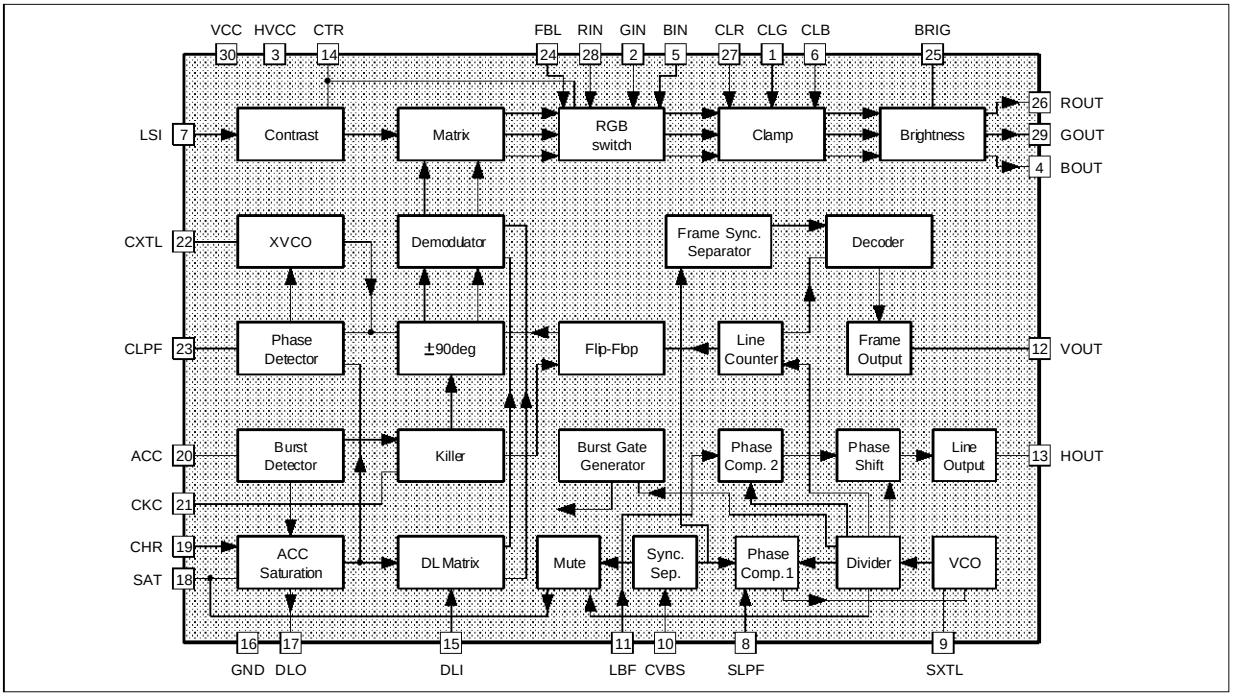
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

DEFLECTION

Synchronization Separator

The synchronization separator is based on the bottom of synchronization pulses alignment to an internal reference voltage. An external capacitor permits to align syncro. pulses, two external resistors determines the detection threshold of synchro pulses.

The frame synchronization pulses are locked to a 32µs reference signal to perfect interlacing.

Horizontal Scanning

The horizontal scanning frequency is obtained from a 500kHz VCO. The circuit uses two phase-locked loops (PLL). The first one controls the frequency, the second one, fully integrated, controls the relative phase of the synchronisation and the line flyback signals.

The first PLL has two time constants : a long time constant during the picture to have a good noise immunity, a short time constant at the beginning of the frame to recapture faster the phase in case of VCR video signal.More over, the PLL is in short time constant three lines before frame pulses occured, it permits to ensure good interlacing when the video signal comes from a VCR tape with high phase error.

The horizontal output signal is 28µs width. On starting up, horizontal pulses are enabled at V_{CC} = 6.8V. On shutting down, horizontal pulses are inhibited for V_{CC} = 6.2V .

The vertical output signal is 10.5 lines width. It permits to drive a sawtooth generator like TDA1771.

A video recognition function permits to sent the information of no video identification to SAT pin : it forces a low level voltage on this pin.

CHROMA

ACC Amplifier, DL Matrix and Demodulators

The ACC amplifier envolves three gain stages : the first one controlled by saturation control voltage, the second one controlled by contrast control voltage, the third one controlled by ACC control voltage. The second stage permits to have a good tracking between the luminance and chrominance signals. The dynamic range of ACC is over than 30dB. The burst signal is not affected by contrast and saturation gain stages. The chrominance output signal is fed to the external delay line.

Then the adding and substraction of the direct and delayed signals are performed by the DL matrix function. The outputs signals U and V are fed to U and V demodulators which consist in two synchronous dectectors. The U demodulator multiplies the (B-Y) signal with the 0^o, 4.43MHz reference signal. The V demodulator multiplies the (R-Y) signal with the alternative $\pm 90^o$,4.43MHz reference signal.

4.43MHz Phase Locked Loop

The oscillating frequency of the 4.43Mhz crystal oscillator is controlled by the output voltage of the loop filter. The phase detector will lock the 90^o reference signal to the direct burst signal. A 90^o phase shifter permits to recover the 0^o reference signal. A flip-flop driven by line pulses permits to generate the alternative $\pm 90^o$ signal.

ACC Control and Color Killer

The direct burst signal is demodulated with the $\pm 90^o$ reference signal. The demodulation result is used both by ACC control and killer functions.

If the demodulation result is always positive, the killer capacitor is charged and the PAL signal is identified (color ON).

When demodulation result is always negative, the killer capacitor is discharged, when the voltage across the capacitor reaches the flip-flop inhibition level, the alternance of $\pm 90^o$ signal is reversed, then the reference signal is in phase with alternative burst and the killer capacitor is charged again.

In case of no video signal, the killer voltage is maintained to a middle voltage below color OFF threshold.

The ACC control voltage is obtained by the peak detection of the demodulated output signal.

VIDEO

The luminance input is controlled by the contrast control stage which range is 20dB.

The luminance and color difference signals are added in the video matrix circuit to obtain the color signals.

The color signals are sent to a RGB switch which will drive to the outputs either internal RGB signals or external RGB signals. With a second threshold on fast blanking input, it is possible to blank the RGB outputs and thus to connect RGB On Screen Display signals directly on the outputs.

The RGB inputs are controlled by a 12dB range contrast control stage.

The black levels are controlled thanks three external capacitors. To avoid the black level of the inserted signal differing from the black level of the normal video signal, the external RGB are clamped to the black level of the luminance signal. Therefore, an AC coupling is required for the RGB inputs.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	12	V
T_{stg}	Storage Temperature	-55, +150	^oC

2100-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	Max.	80	$^oC/W$

2100-02.TBL

DC AND AC ELECTRICAL CHARACTERISTICS (V_{CC} = 9V, T_{amb} = 25^{o}C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
HV_{CC}	Scanning Supply Voltage (Pin 3)		8	9	10	V
V_{CC}	Video & Chroma Supply Voltage (Pin 30)		8	9	10	V
I_{CCh}	Scanning Supply Current (Pin 3)	No load		20	30	mA
$I_{CCv\&c}$	Video & Chroma Supply Current (Pin 30)	No load		30	50	mA
P_D	Total Power Dissipation	No load		450	800	mW
LUMINANCE INPUT (Pin 7)						
V_{BW7}	Input Level before Clipping (black to white)				450	mV_{PP}
V_{DC7}	DC Operating Voltage	No input signal		2.8		V
I_7	Input Current	• During burst period • Out of burst period		± 100	5	µA µA
G_7	Luma Gain			12		
BW_7	Bandwidth	-3dB		5		MHz

2100-03.TBL

DC AND AC ELECTRICAL CHARACTERISTICS (V_{CC} = 9V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CONTRAST CONTROL (Pin 14)						
V_{14}	Contrast Control Voltage			2 to 4		V
G_{14}	Contrast Control Range			20		dB
I_{14}	Input Current				20	µA
BRIGHTNESS CONTROL (Pin 25)						
V_{25}	Brightness Control Voltage			1.5 to 7		V
I_{25}	Input Current				10	µA
RGB OUTPUTS (Pins 26-29-4)						
$V_{BW26-29-4}$	Output Signal Amplitude (black to white)	● 0.35V B to W @ Pin 7 ● Contrast @ max ● Sat. @ min ● Brig. @ 2V		4.2		V
$V_{BLU26-29-4}$	Blue Channel Output Amplitude (No Y)	● At Pin 19 (B-Y) signal : 300mV$_{PP}$ with burst amplitude 300mV ● Contrast @ typ ● Sat. @ typ ● Brig. @ 4V		5.6		V_{PP}
$I_{26-29-4}$	Individual Output Sinking Current			2		mA
$V_{M26-29-4}$	Maximum Peak White Level			8		V
$V_{blank\ 26-29-4}$	Blanking Level			0.7		V
$\Delta V_{26-29-4}$	Difference in the Black Level between the three Channels			50	500	mV
ΔV_{CTR}	Variation of Black Level with Contrast				120	mV
ΔV_{REL}	Relative Black Level Variation between the three Channels during Variation of CTR (10dB), BRIG (± 1V), V_{CC} (± 10%)				20	mV
$\Delta V_{video-RGB}$	Difference between Black Level of Video and Inserted Signal at the Output				200	mV
ΔV_{temp}	Black Level Thermal Drift			0.5		mV/°C
REJ1	Crosstalk External RGB → Video	1MHz		-50		dB
REJ2	Crosstalk Video → External RGB	1MHz		-50		dB
RGB CLAMP CAPACITORS (Pins 27-1-6)						
I_{27-1-6}	Control Current			± 100		µA
$I_{l\ 27-1-6}$	Leakage Current				5	µA
RGB INPUTS (Pins 28-2-5)						
$V_{BW28-2-5}$	Maximum Input Level (B to W)				2	V
$V_{clamp28-2-5}$	Clamp Level	Contrast max		2.9		V
BW_{28-2-5}	Bandwidth	-3dB		8		MHz
G_{CTR}	RGB Contrast Control Range			12		dB
G_{28-2-5}	RGB Gain			6		
FAST BLANKING INPUT (Pin 24)						
V_{TH1-24}	First Threshold (switching)			0.7		V
V_{TH2-24}	Second Threshold (switching)			2.1		V
I_{24}	Input Current	0V @ Pin 24			100	µA
T_{switch}	Switching Delay			50		ns
T_{blank}	Blanking Delay			50		ns
CHROMINANCE INPUT (Pin 19)						
V_{19}	Input Level before Clipping				900	mV_{PP}
$V_{burst-19}$	Minimum Burst Signal Amplitude within the ACC Control Range			30		mV_{PP}

2100-04.TBL

DC AND AC ELECTRICAL CHARACTERISTICS (V_{CC} = 9V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CHROMINANCE INPUT (Pin 19) (continued)						
G_{ACC}	ACC Control Range	Change of burst over whole ACC control range < 1dB	30			dB
R_{19}	Input Impedance			8		k
V_{DC-19}	DC Operating Voltage	No input signal		2.8		V
SATURATION CONTROL INPUT (Pin 18)						
I_{18}	Input Current				10	µA
SAT-CTR	Tracking between Luminance and Chrominance Signals over 10dB Contrast Control				2	dB
V_{low-18}	Low Level when no Video Recognition			100		mV
ACC CAPACITOR (Pin 20)						
I_{20}	Charging Current	During burst gate period		200		µA
I_{l20}	Leakage Current	Out of burst gate period			5	µA
KILLER CAPACITOR (Pin 21)						
V_{OFF-21}	Collor off Voltage	No chroma signal		4.9		V
V_{ON-21}	Color on Voltage			5.4		V
V_{INH-21}	PAL Flip-flop Inhibition Level			3.2		V
I_{21}	Control Current			200		µA
I_{l21}	Leakage Current				5	µA
V_{nom-21}	Voltage with Nominal Input Signal			6.0		V
PLL LOOP FILTER (Pin 23)						
I_{23}	Control Current			800		µA
I_{l23}	Leakage Current				5	µA
CHROMA XTAL (Pin 22)						
CR_{22}	Catching Range			700		Hz
SUBCARRIER OUTPUT (Pin 17)						
$V_{burst-17}$	Output Burst Amplitude	Within ACC control range		2.6		V_{PP}
DELAYED CHANNEL INPUT (Pin 15)						
V_{DC-15}	DC Operating Voltage	No input signal		2.2		V
R_{15}	Input Impedance			8		k
COMPOSITE VIDEO BASE BAND SIGNAL (Pin 10)						
V_{REF-10}	Voltage Reference	I_{10} = -1µA	0.6	0.8	1.0	V
V_{10}	Video Input Signal				2.5	V_{PP}
SCANNING VCO (Pin 9)						
F_9	Frequency after Divider			15.625		kHz
CR_9	Frequency Control Range after Divider			± 700		Hz
PLL LOOP FILTER (Pin 8)						
I_{low-8}	Output Current Low Loop Gain			0.15		mA
I_{high-8}	Output Current High Loop Gain			0.40		mA
LINE FLYBACK INPUT (Pin 11)						
V_{TH-11}	Threshold			0		V
V_{11}	Line Flyback Amplitude		0.8			V_{PP}
V_{DC-11}	Minimum DC Voltage		-0.4			V
I_{11}	Input Current				5	µA
$D_{11/26-28-4}$	Delay between LFB Pulse and Line Blanking on RGB Outputs			200		ns

2100-05.TBL

DC AND AC ELECTRICAL CHARACTERISTICS (V_{CC} = 9V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
HORIZONTAL OUTPUT (Pin 13)						
T_{13}	Output Pulse Width		26	28	29	µs
V_{low-13}	Output Voltage (open collector)	I_{13} = 10mA		1		V
$V_{start-13}$	V_{CC} Start Level			6.8		V
$V_{stop-13}$	V_{CC} Stop Level			6.2		V
Δt_{13}	φ2 Phase Range			10		µs
VERTICAL OUTPUT (Pin 12)						
T_{12}	Output Pulse Width			10.5		lines
T_{sync}	Frame Synchro. Window			248 to 352		line
V_{low-12}	Output Voltage (open collector)	I_{12} = 10mA		1		V

2100-06.TBL

Figure 1 : Pins 1-6-27-25 (CLG, CLB, CLR, BRIG)

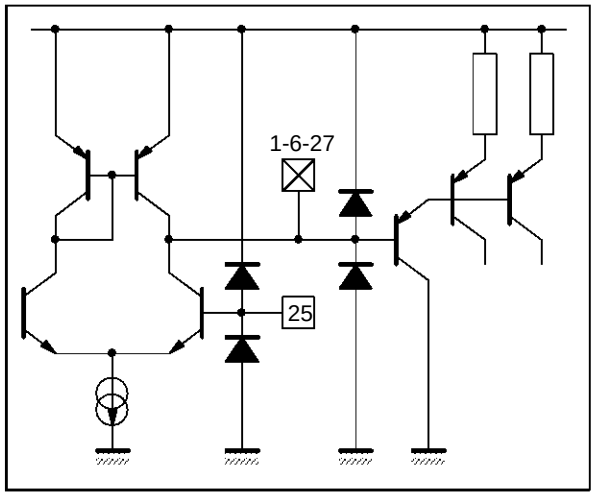


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Figure 2 : Pins 2-5-28 (G_{IN}, B_{IN}, R_{IN})

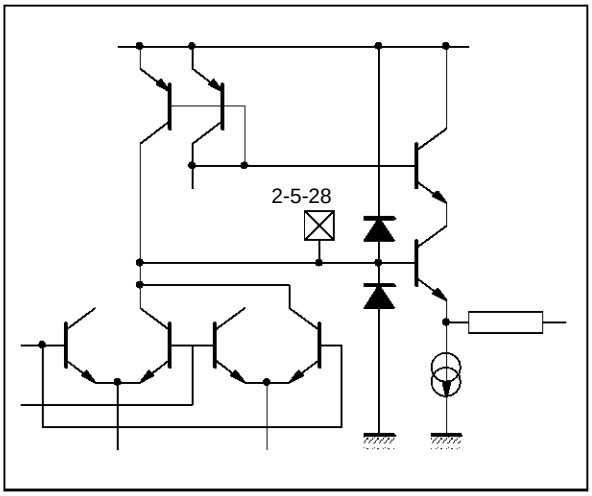

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Figure 3 : Pins 4-29-26 (B_{OUT}, G_{OUT}, R_{OUT})

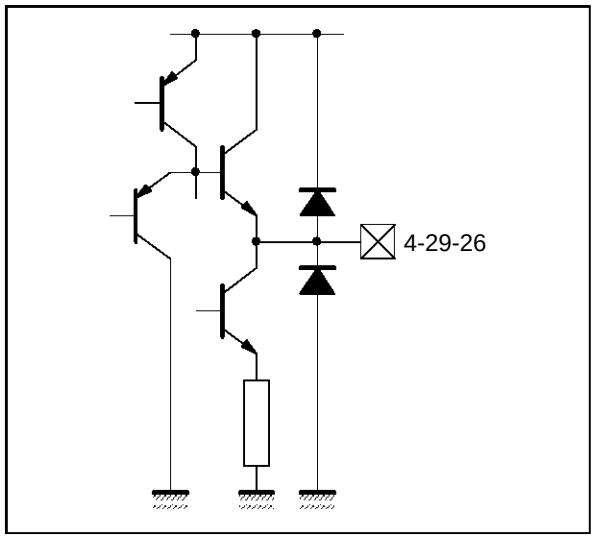

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Figure 4 : Pin 7 (LSI)

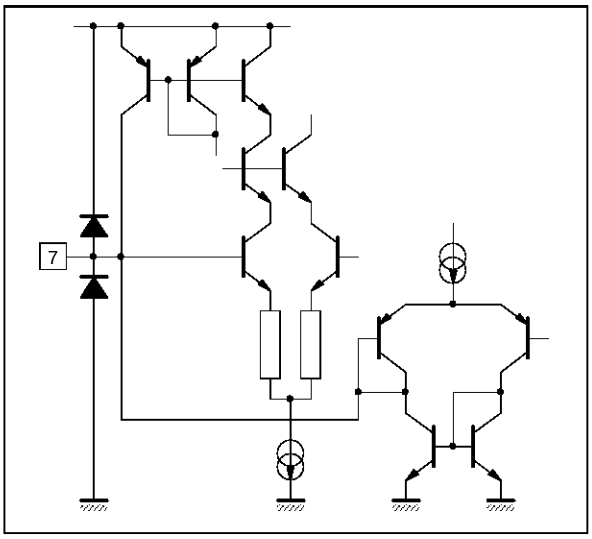

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Figure 5 : Pin 8 (SLPF)

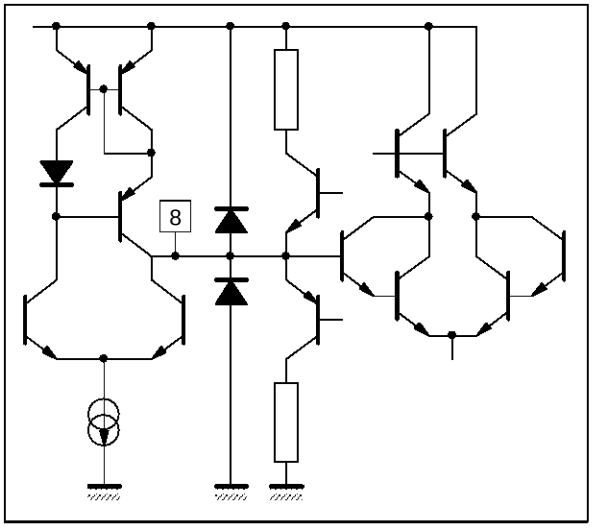


Figure 6 : Pin 9 (SXTL)

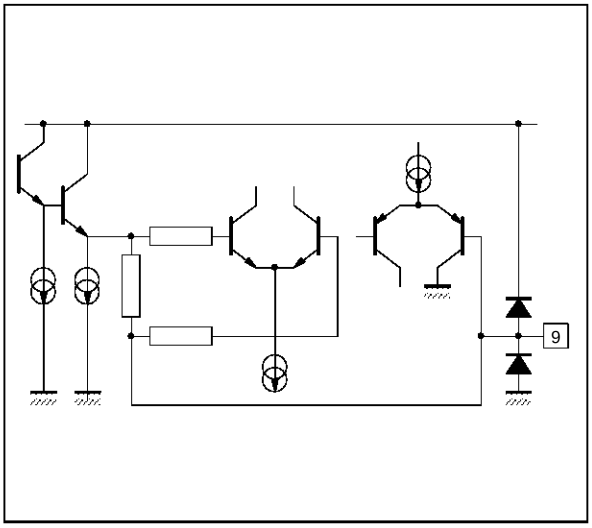


Figure 7 : Pin 10 (CVBS)

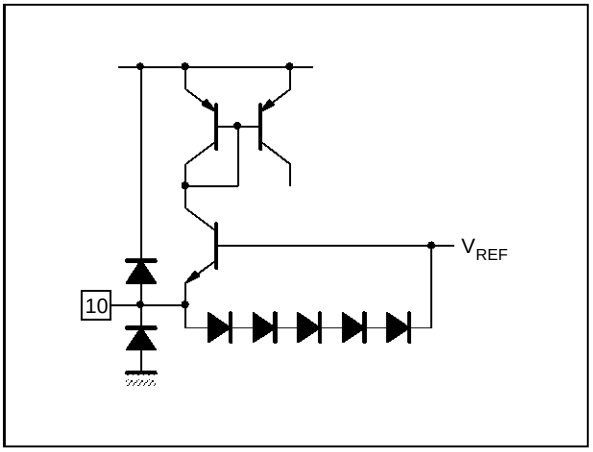


Figure 8 : Pin 11 (LFB)

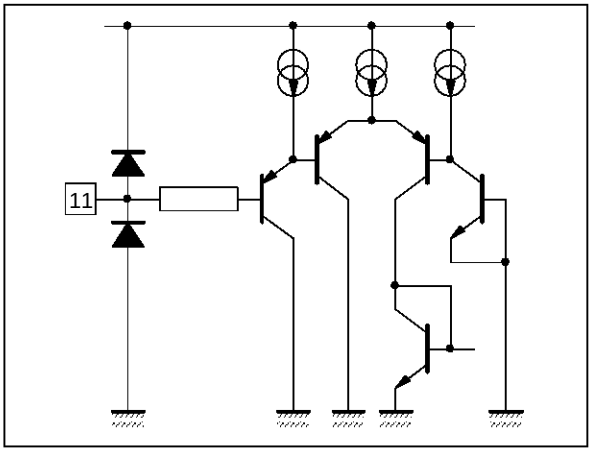


Figure 9 : Pins 12-13 (V_{OUT}, H_{OUT})

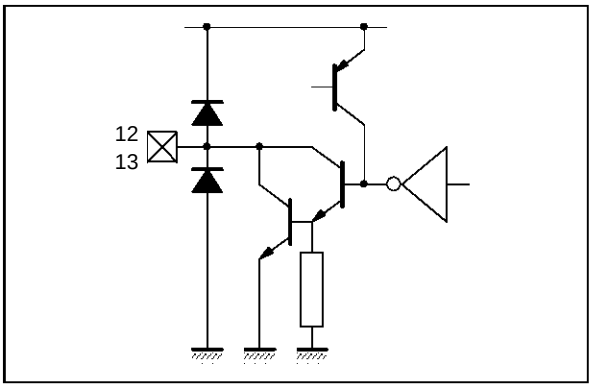


Figure 10 : Pin 14 (CTR)

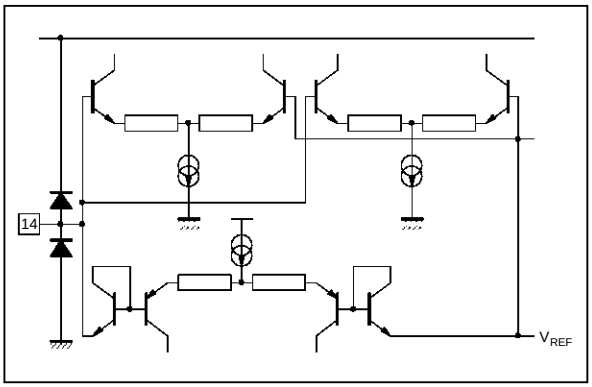


Figure 11 : Pin 15 (DLI)

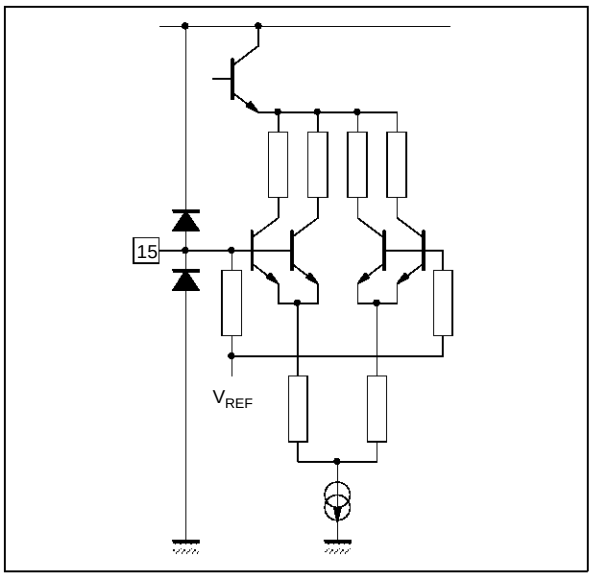


Figure 12 : Pin 17 (DLO)

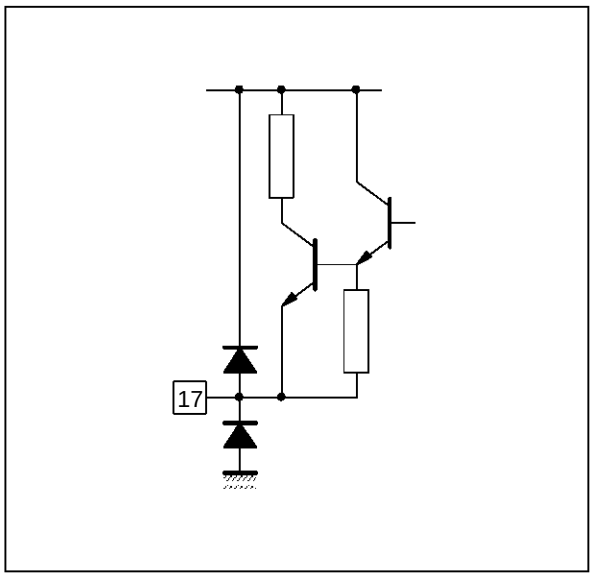


Figure 13 : Pin 18 (SAT)

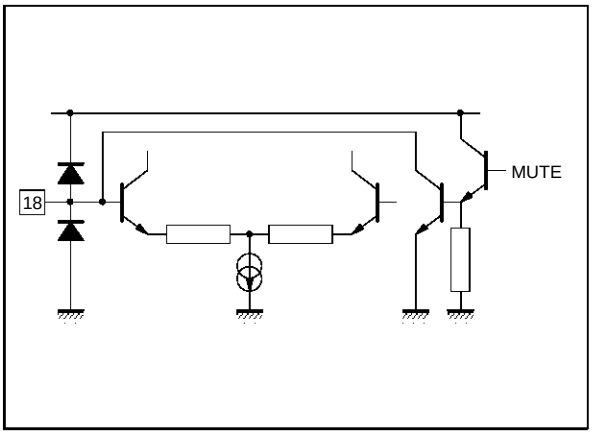


Figure 14 : Pin 19 (CHR)

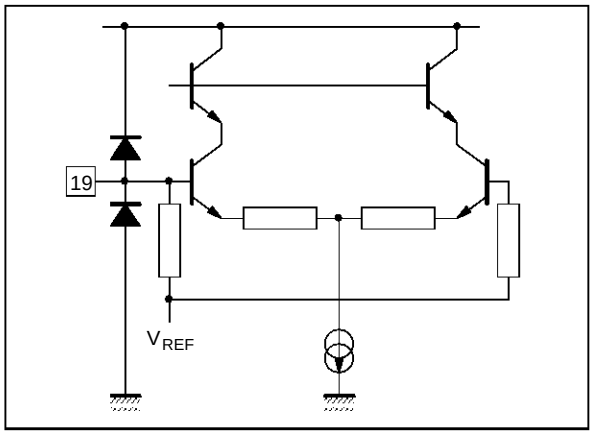


Figure 15 : Pin 120 (ACC)

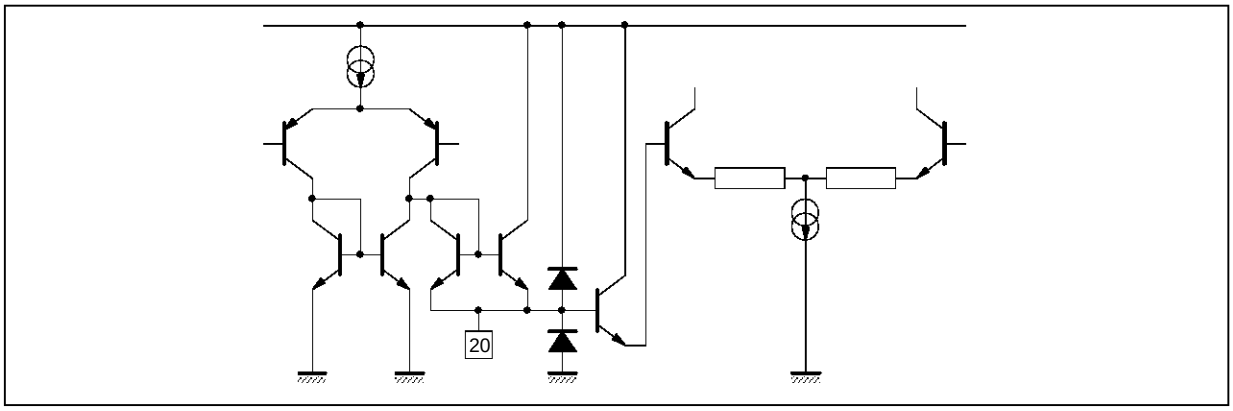


Figure 16 : Pin 21 (CKC)

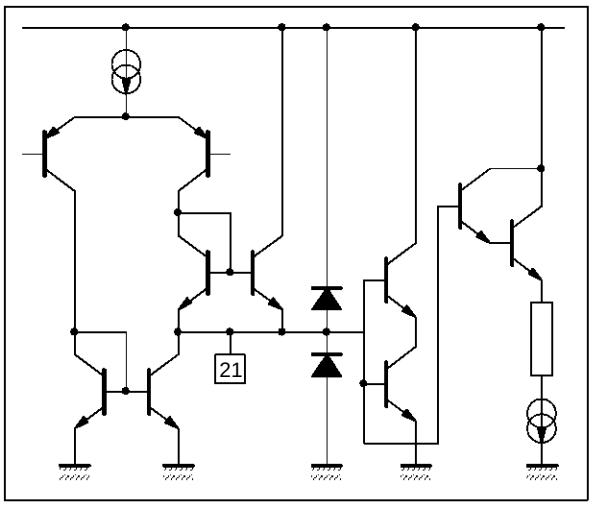


Figure 17 : Pin 22 (CXTL)

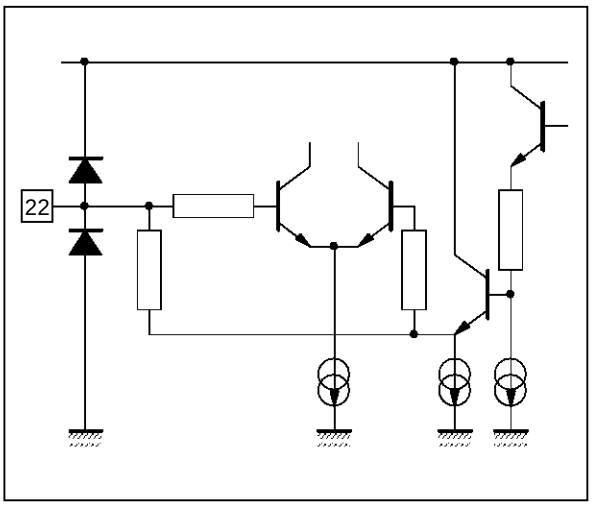


Figure 18 : Pin 23 (CLPF)

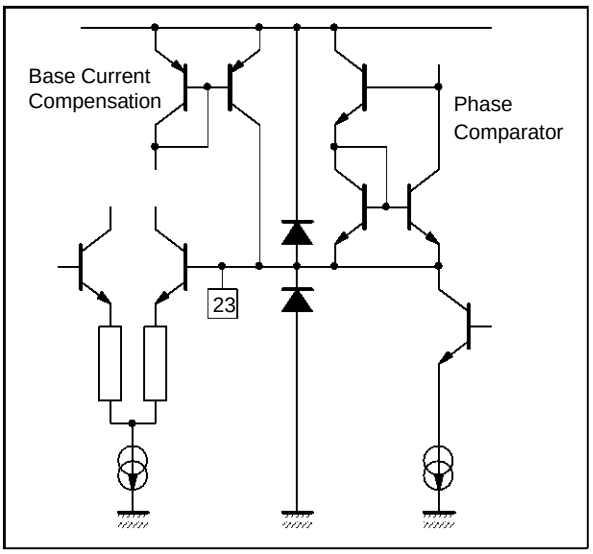
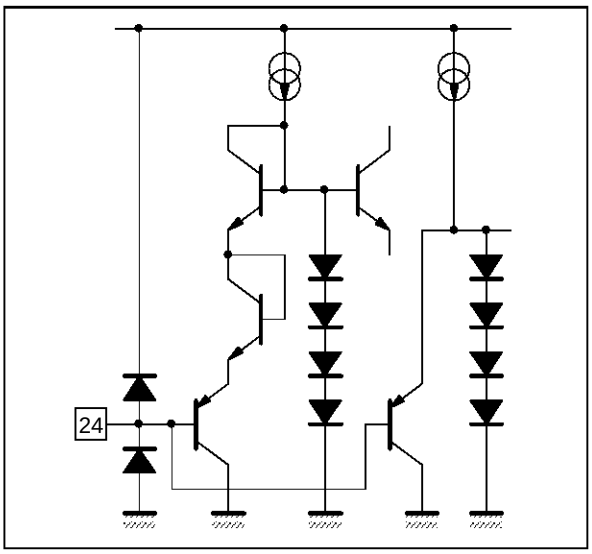
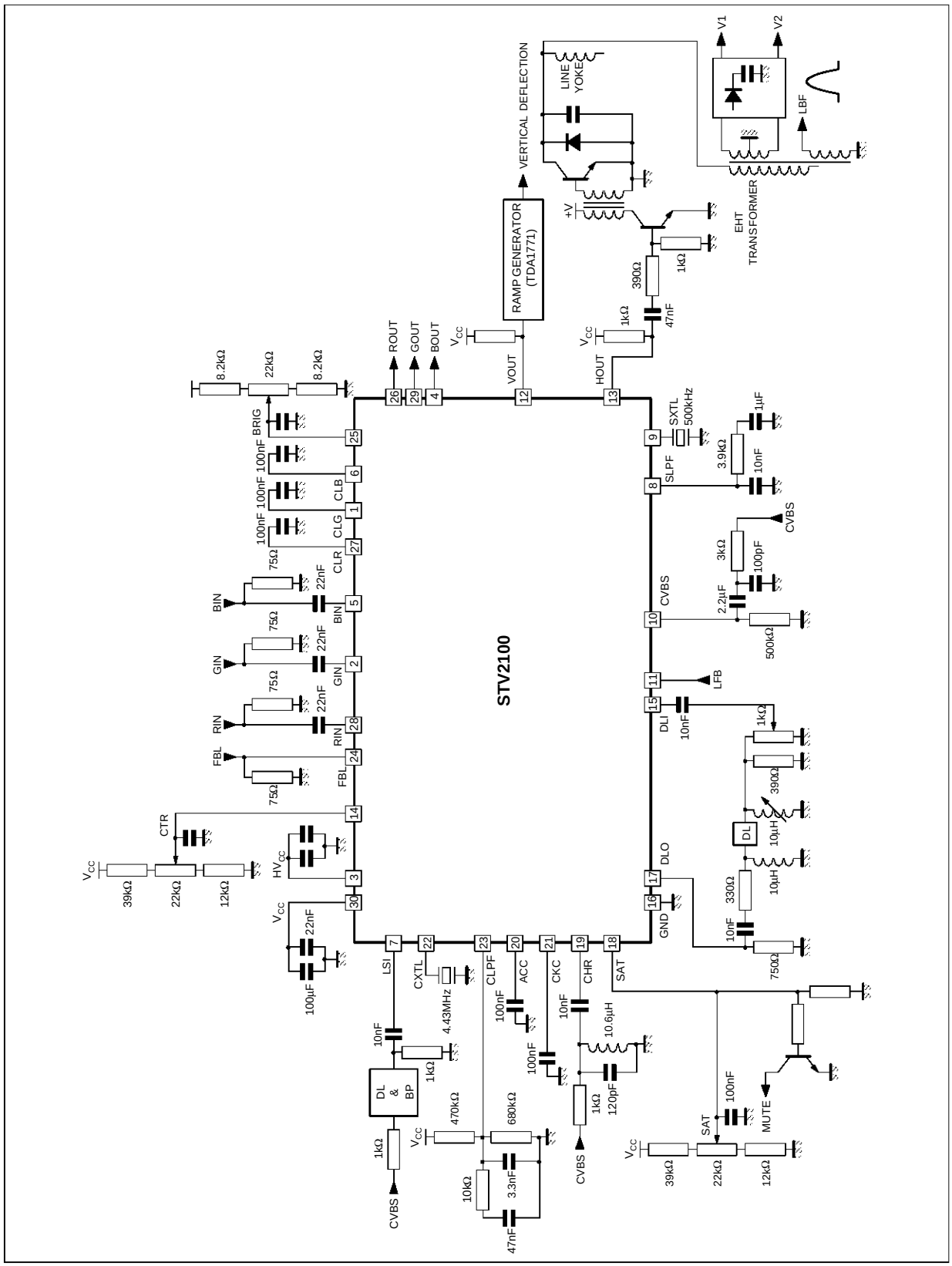


Figure 19 : Pin 24 (FBL)

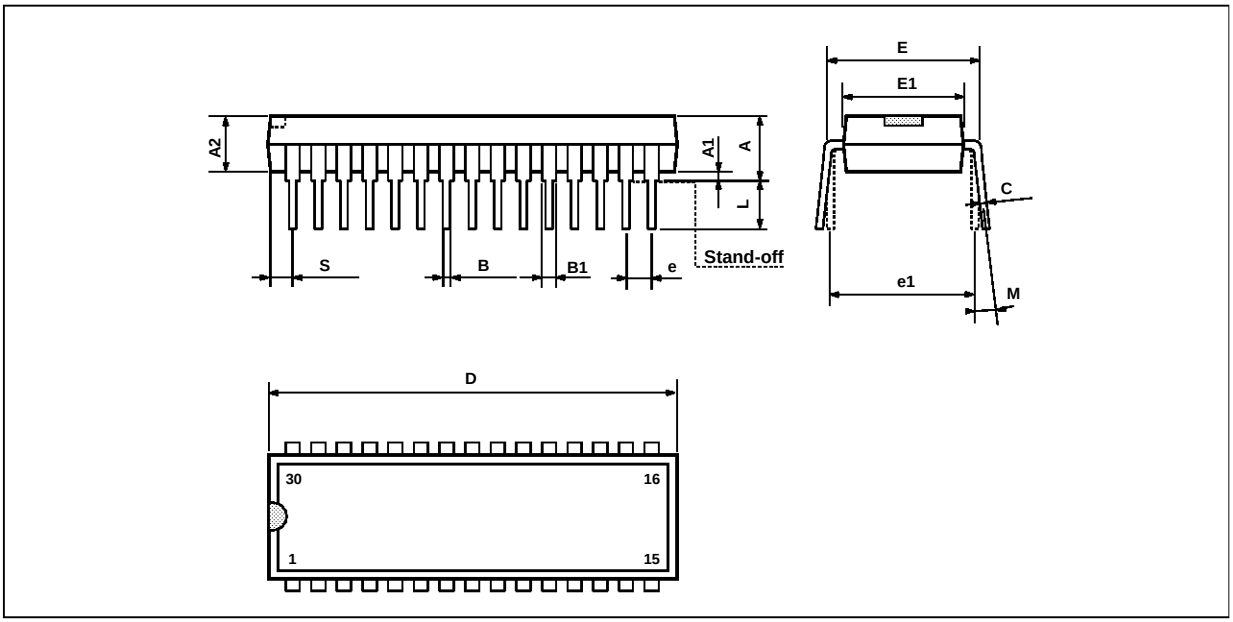


APPLICATION DIAGRAM



PACKAGE MECHANICAL DATA

30 PINS - PLASTIC SHRINK



PMSDIP30.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.08			0.20
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.12	0.15	0.18
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	0.76	0.99	1.40	0.030	0.039	0.055
C	0.20	0.25	0.36	0.008	0.01	0.014
D	27.43	27.94	28.45	1.08	1.10	1.12
E	10.16	10.41	11.05	0.400	0.410	0.435
E1	8.38	8.64	9.40	0.330	0.340	0.370
e		1.78			0.070	
e1		10.16			0.400	
L	2.54	3.30	3.81	0.10	0.13	0.15
M	0^o (min.), 15^o (max.)					
S	0.31			0.012		

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